

MS-7085

Version 0B

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CPU:

Intel LGA775 CPU

System Chipset:

Intel 915GV (North Bridge)

Intel ICH6 (South Bridge)

On Board Chipset:

BIOS -- FWH EEPROM

AC'97 Codec -- ADI1981B

LPC Super I/O -- SMSC LPC47M287

LAN -- Realtek 8101L

CLOCK -- ICS954119

Main Memory:

DDR 1 * 2 (Max 2GB)

Expansion Slots:

PCI SLOT * 1

Intersil PWM:

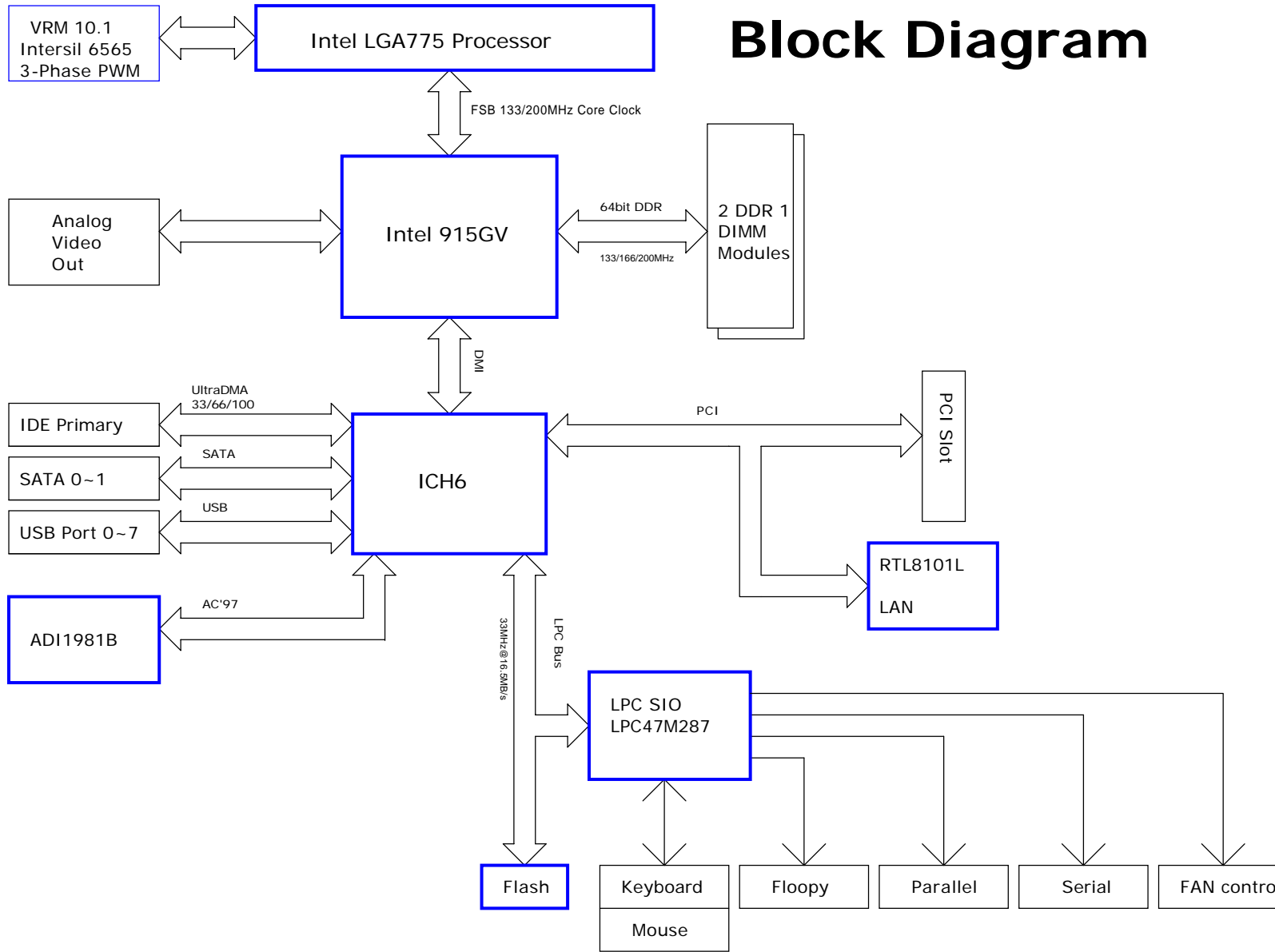
Controller: HIP6565 3 Phase

Driver: HIP6602B * 1 + HIP6601B * 1

PCI Routing Table

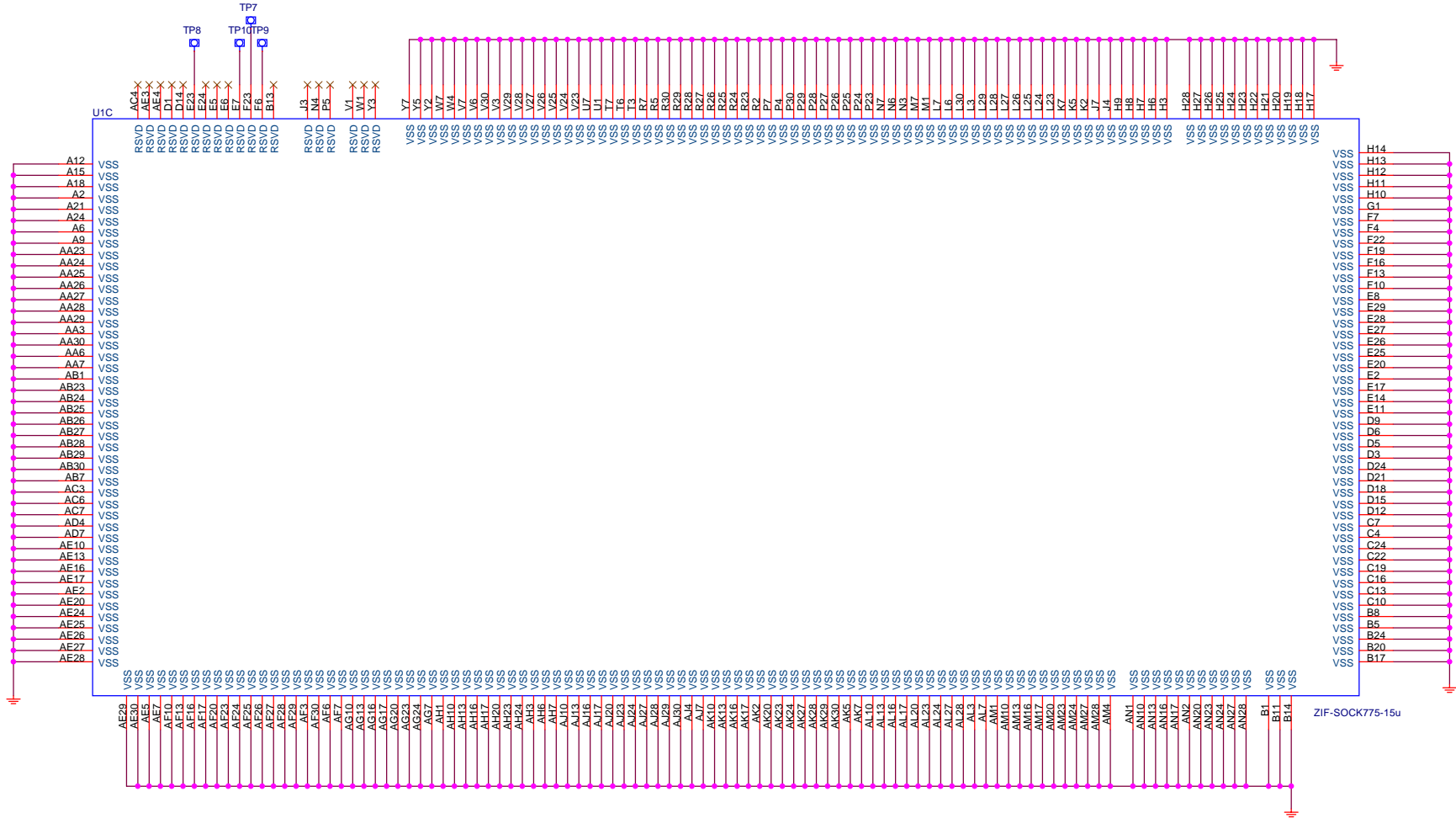
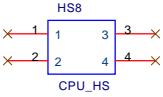
PCI Device	IDSEL	REQ/GNT	INTERRUPT
PCI Slot 1	AD16	1	A
RTL8101L LAN	AD29	3	F

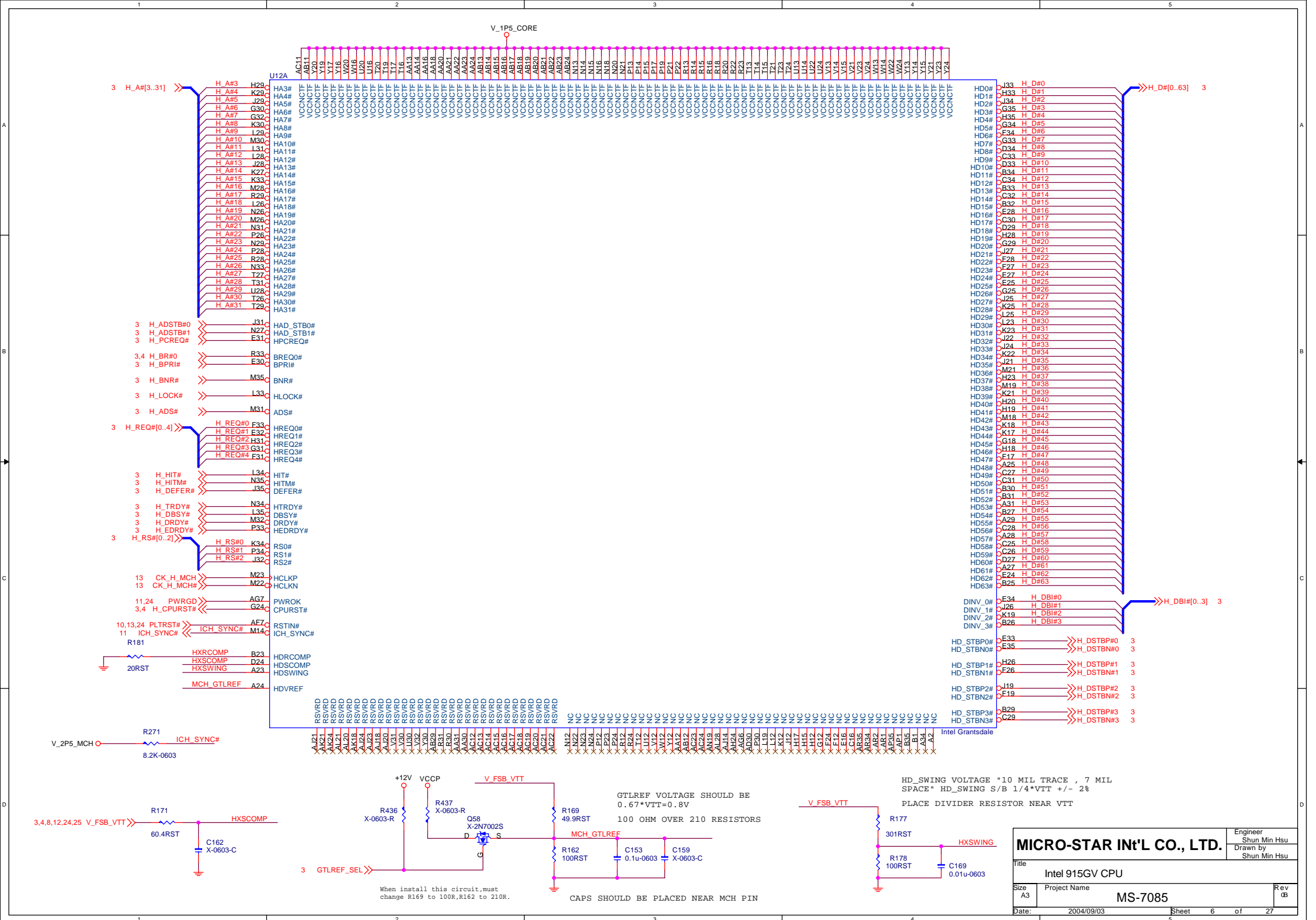
MICRO-STAR INT'L CO., LTD.		Engineer Shun Min Hsu
Title COVER SHEET		Drawn by Shun Min Hsu
Size A3	Project Name MS-7085	Rev (B)
Date: 2004/09/03	Sheet 1	of 27

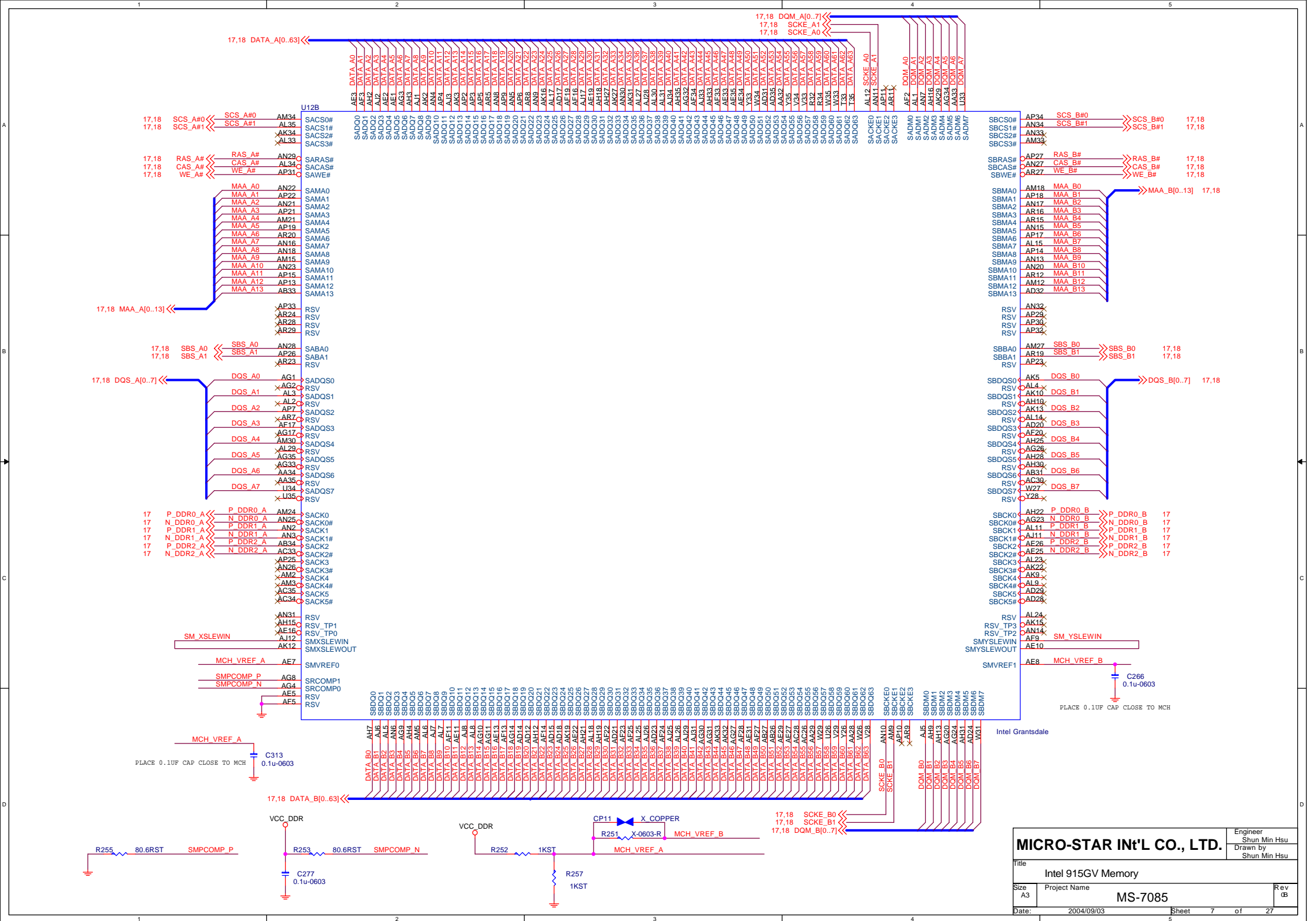


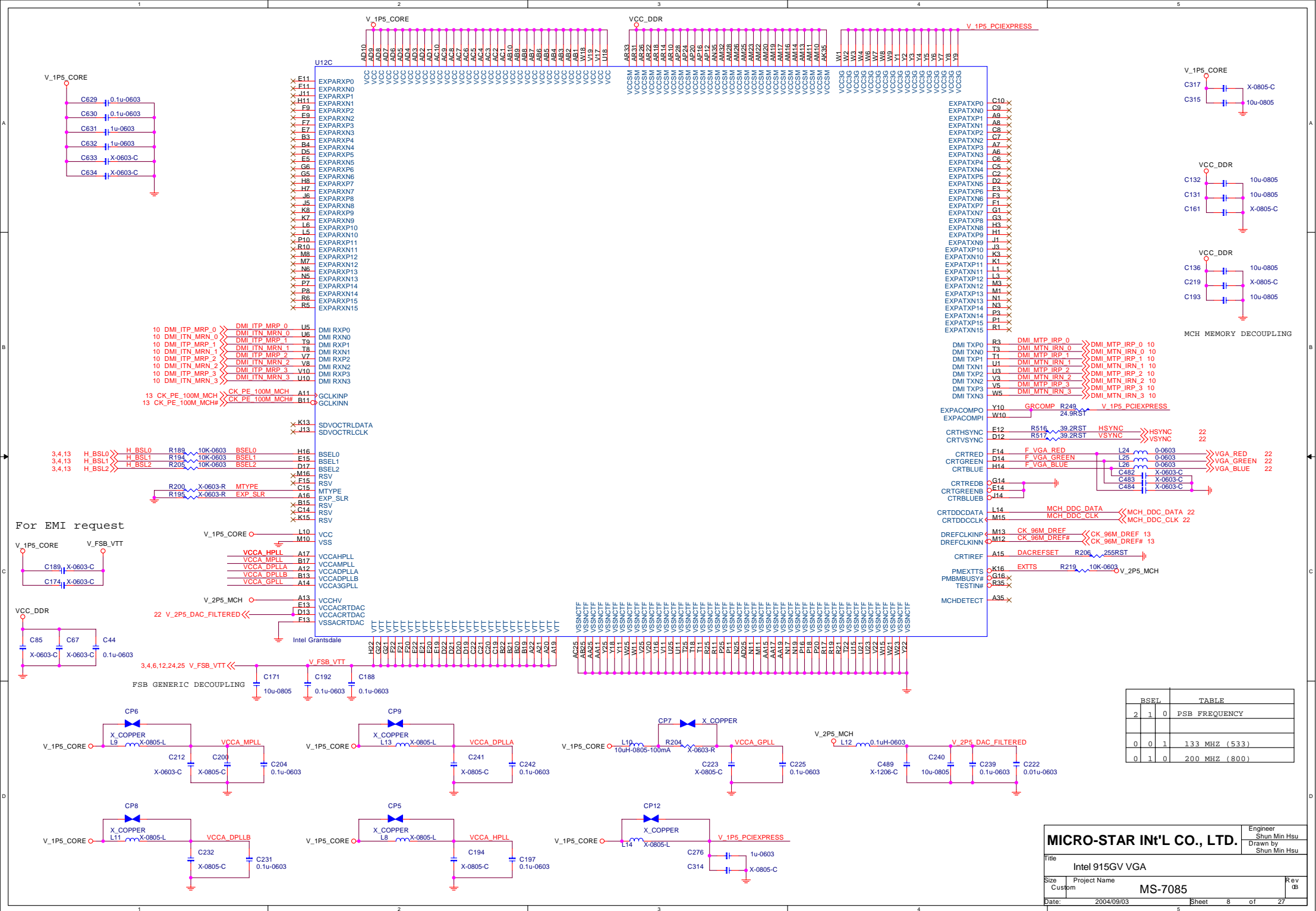
Block Diagram

Rev
03











MICRO-STAR INT'L CO., LTD.			Engineer Shun Min Hsu
Title Intel 915GV GND			Drawn by Shun Min Hsu
Size A3	Project Name MS-7085	Rev (B)	
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U12_41
HS-HOOK-L



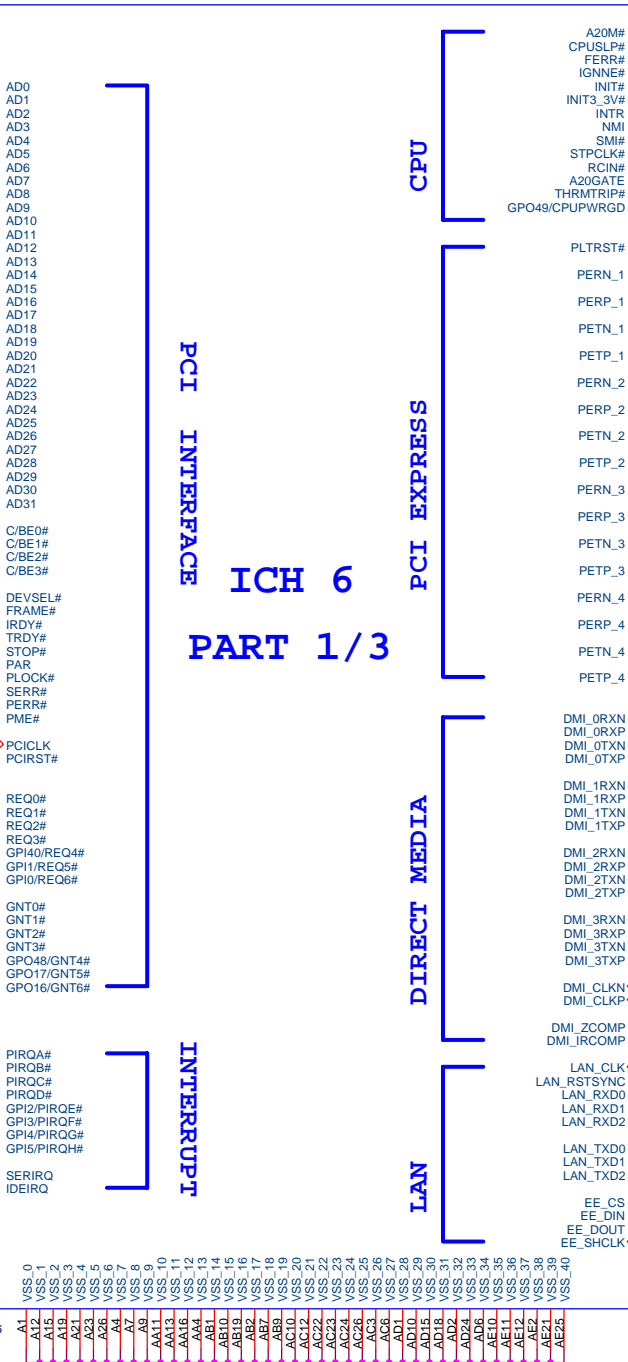
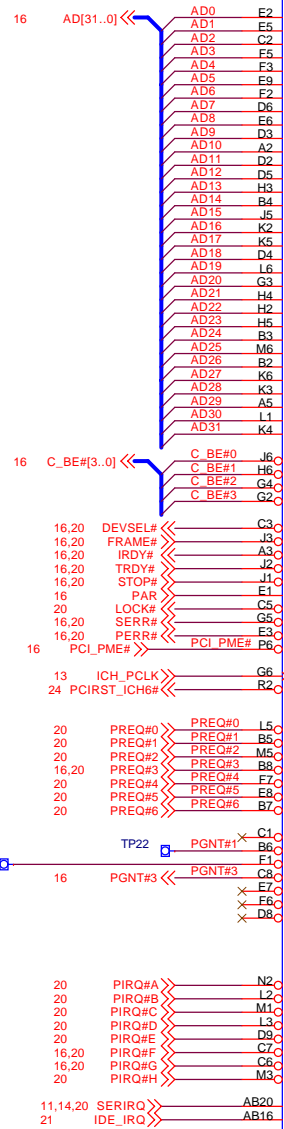
U12_42
HS-HOOK-L



U12_43
HS-HOOK-L



U12_44
HS-HOOK-L



CPU

PCI EXPRESS

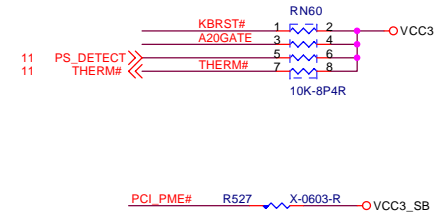
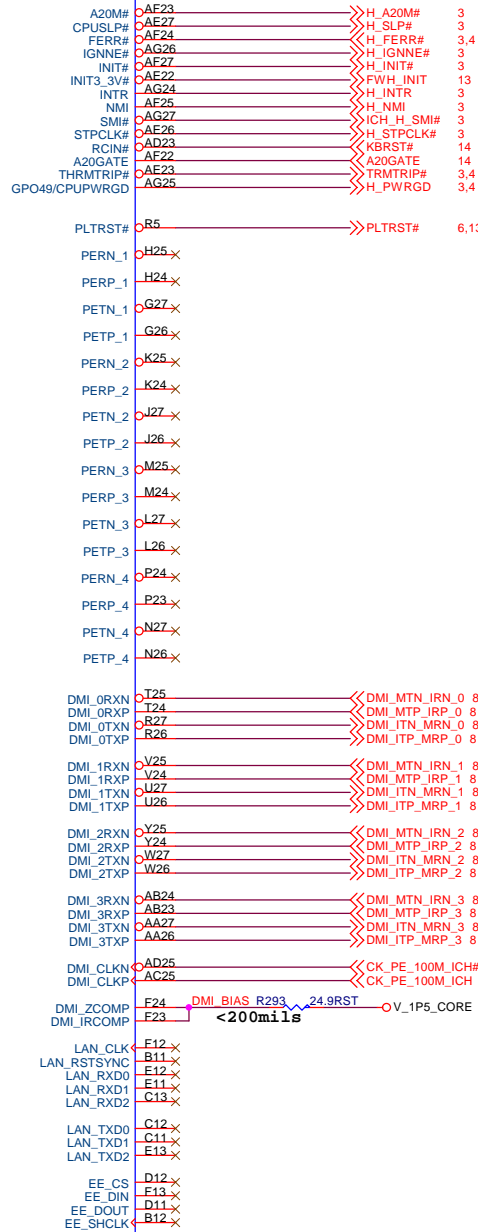
DIRECT MEDIA

LAN

PCI INTERFACE

ICH 6
PART 1/3

INTERRUPT



DMI Interface

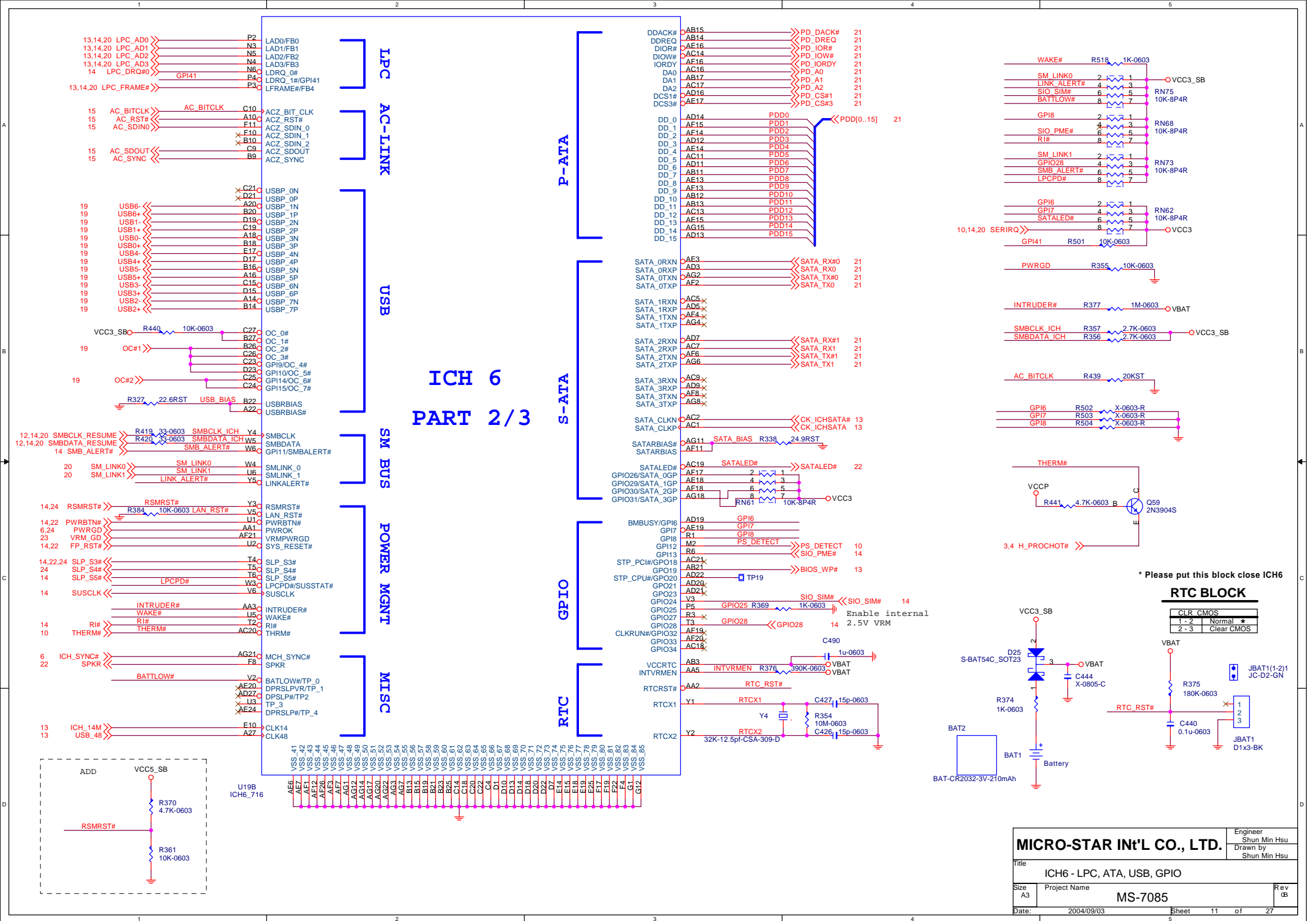
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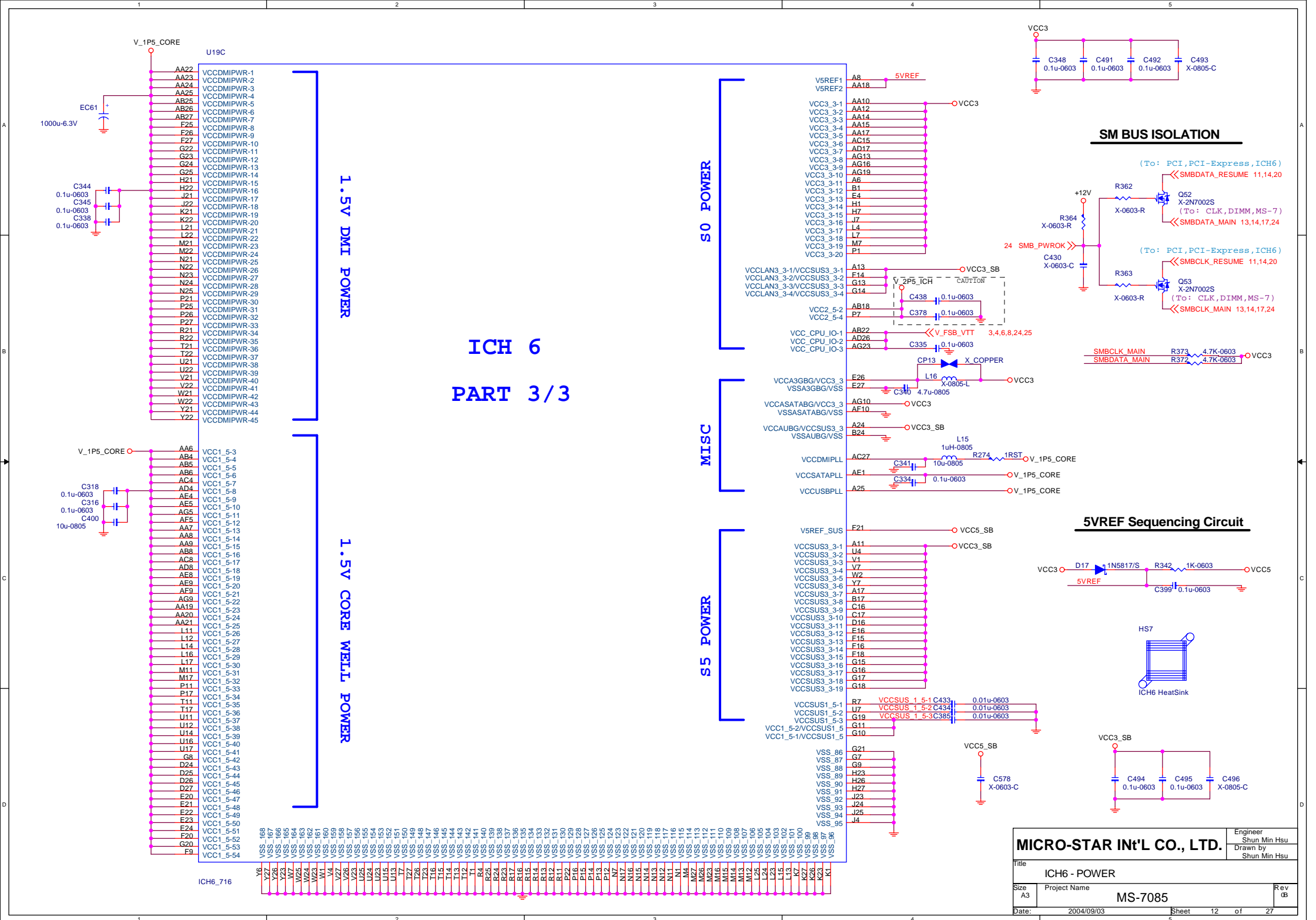
GMCH breakout space 5 mils, length < 250 mils

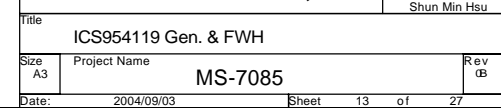
Length matching < 5 mils

Trace Length 2" to 11"

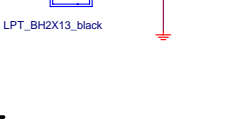
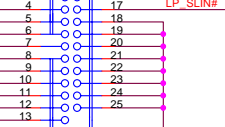
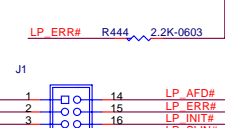
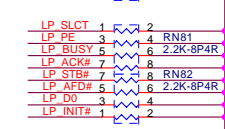
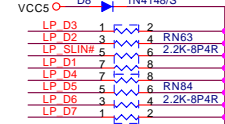
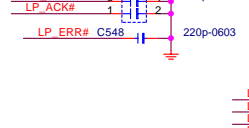
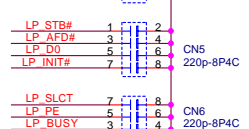
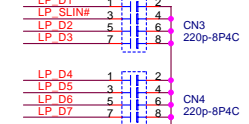
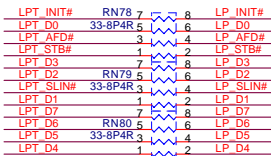
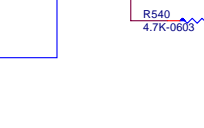
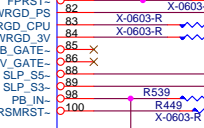
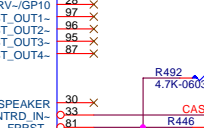
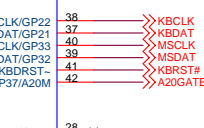
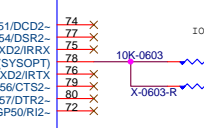
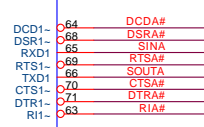
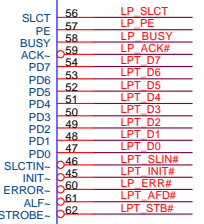
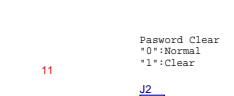
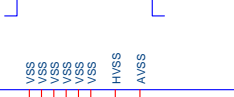
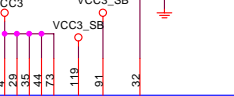
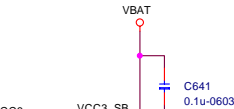
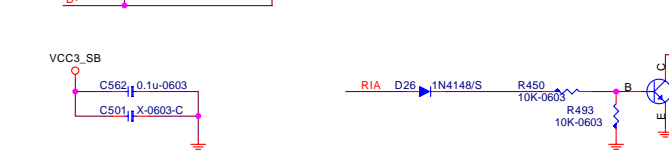
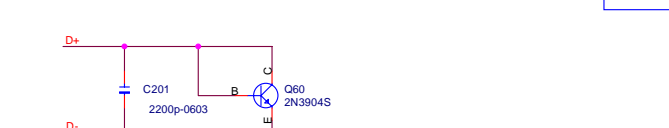
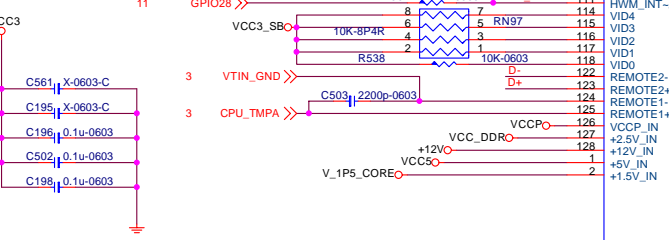
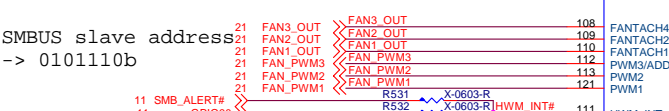
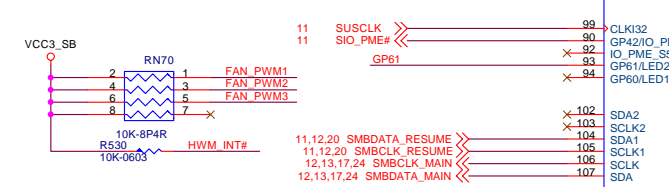
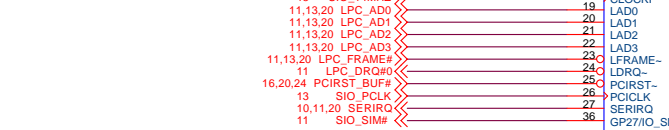
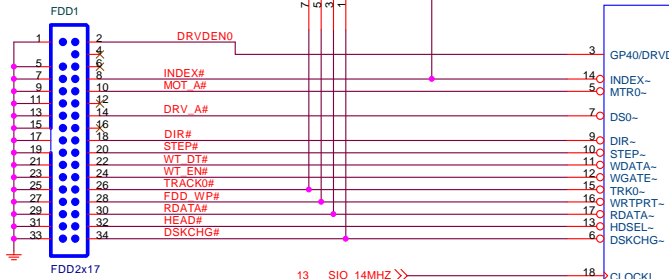
MICRO-STAR INT'L CO., LTD.		Engineer Shun Min Hsu
Title ICH6 - PCI, DMI, CPU, IRQ		Drawn by Shun Min Hsu
Size A3	Project Name MS-7085	Rev (B)
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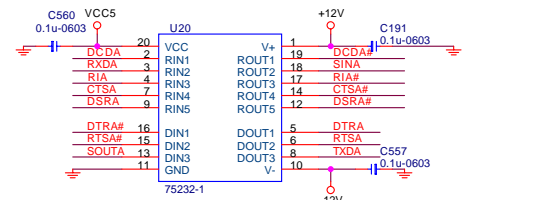




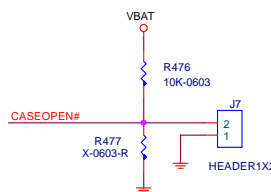
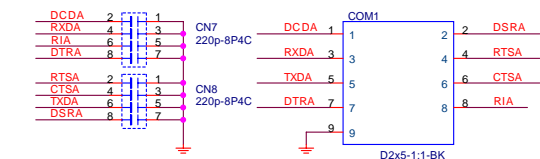
FLOPPY CONNECTOR



SERIAL PORT 1



COM1 HEADER



Password Clear
0:Normal
1:Clear

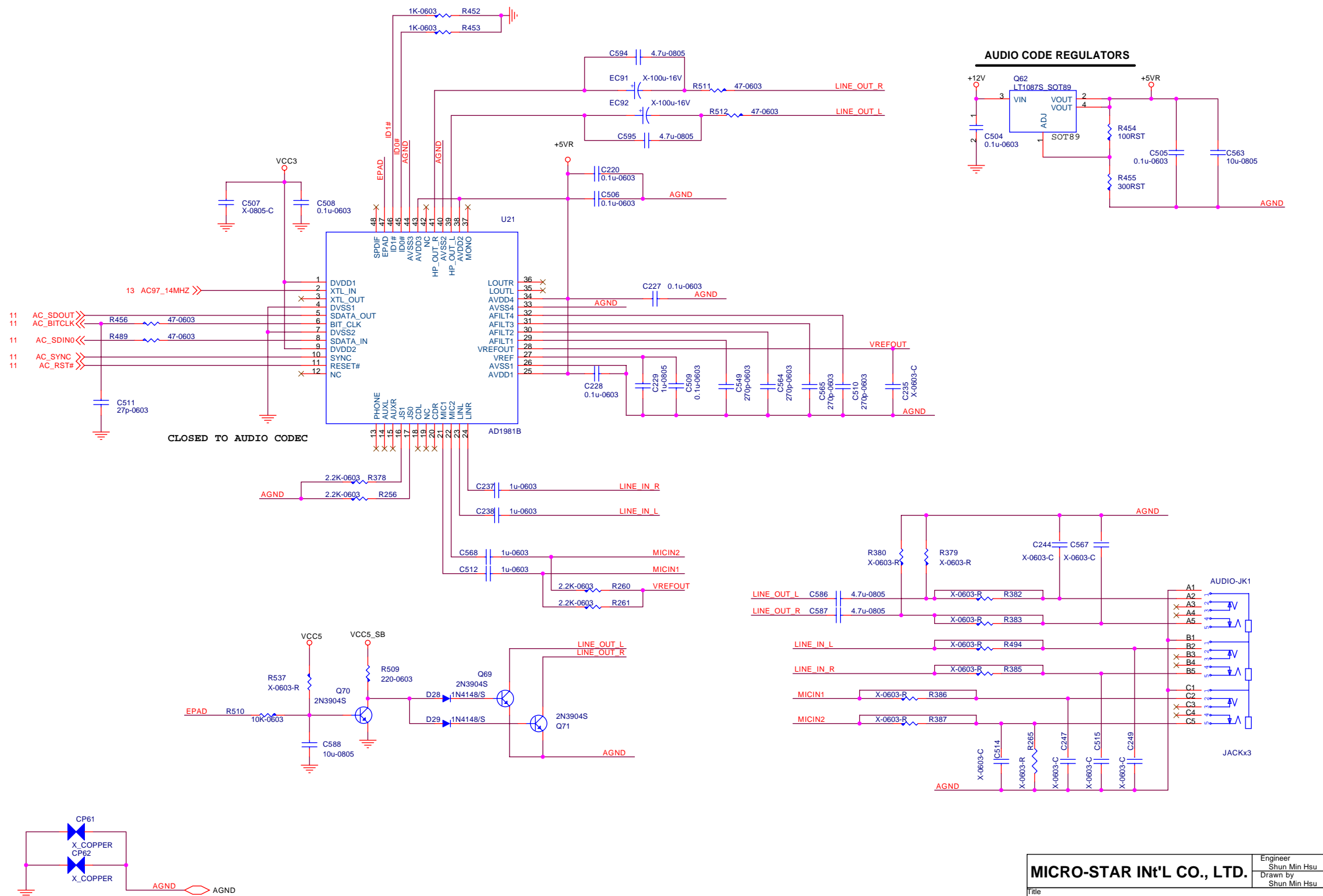
Final Pinout - Rev 0.51 - 11/21/02

Header Pinout - Rev 0.51 - 11/21/02

Header Pinout - Rev 0.51 - 11/21/02

Header Pinout - Rev 0.51 - 11/21/02

MICRO-STAR IN'L CO., LTD.		Engineer Shun Min Hsu
Title LPC47M287		Drawn by Shun Min Hsu
Size Custom	Project Name MS-7085	Rev 0B
Date 2004/09/03	Sheet 14	of 27

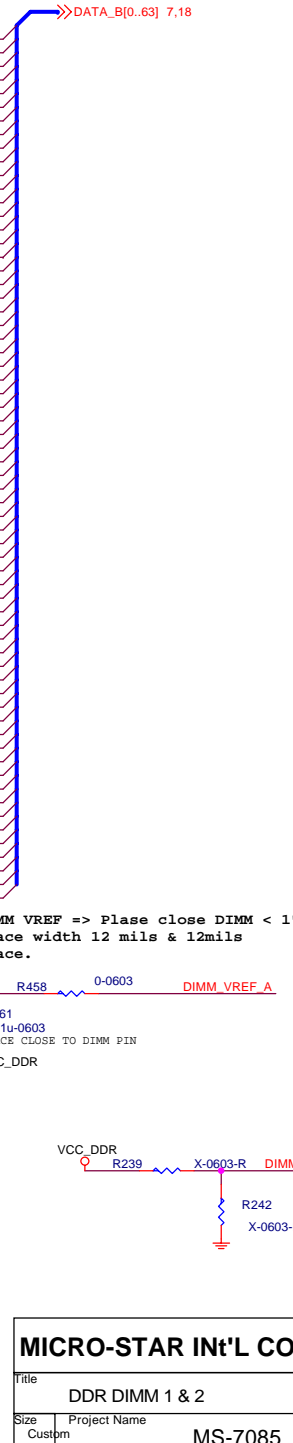
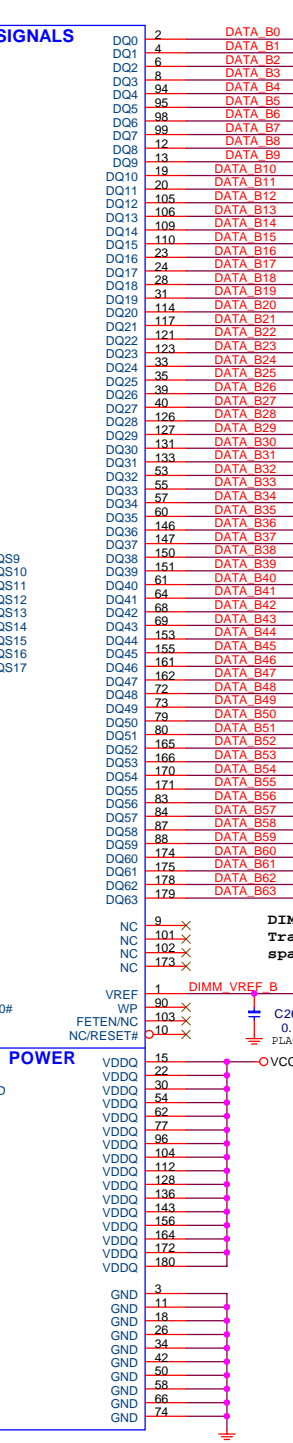
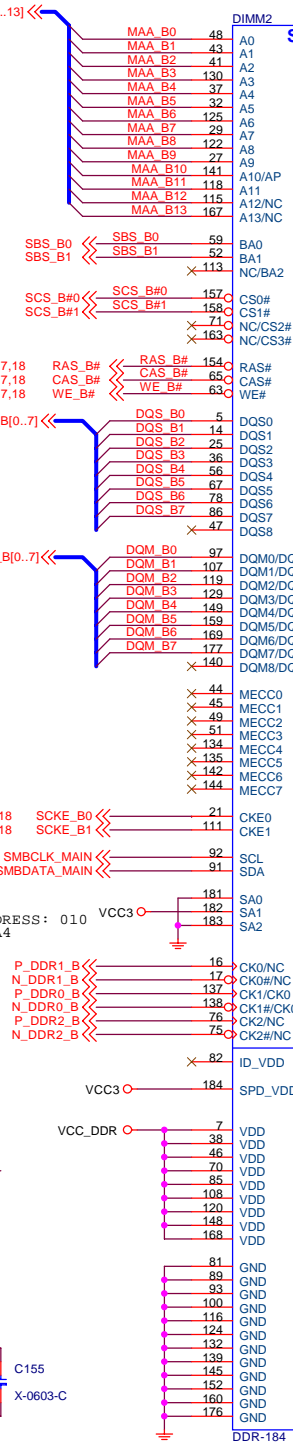
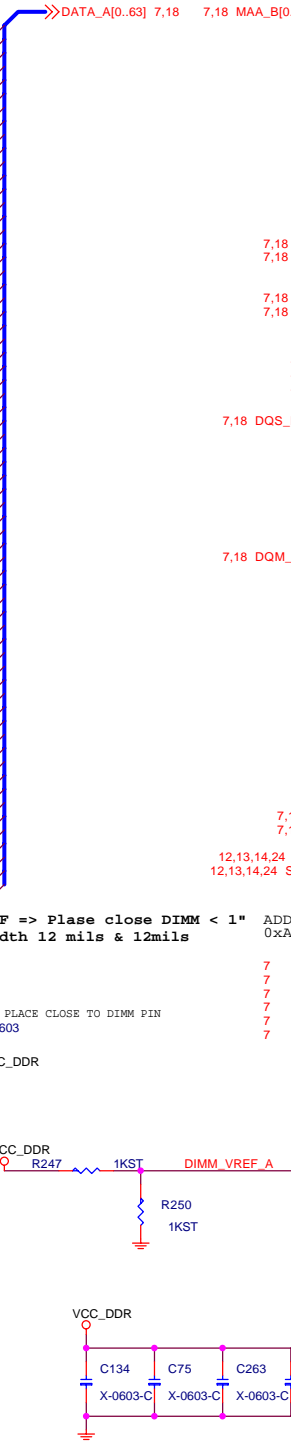
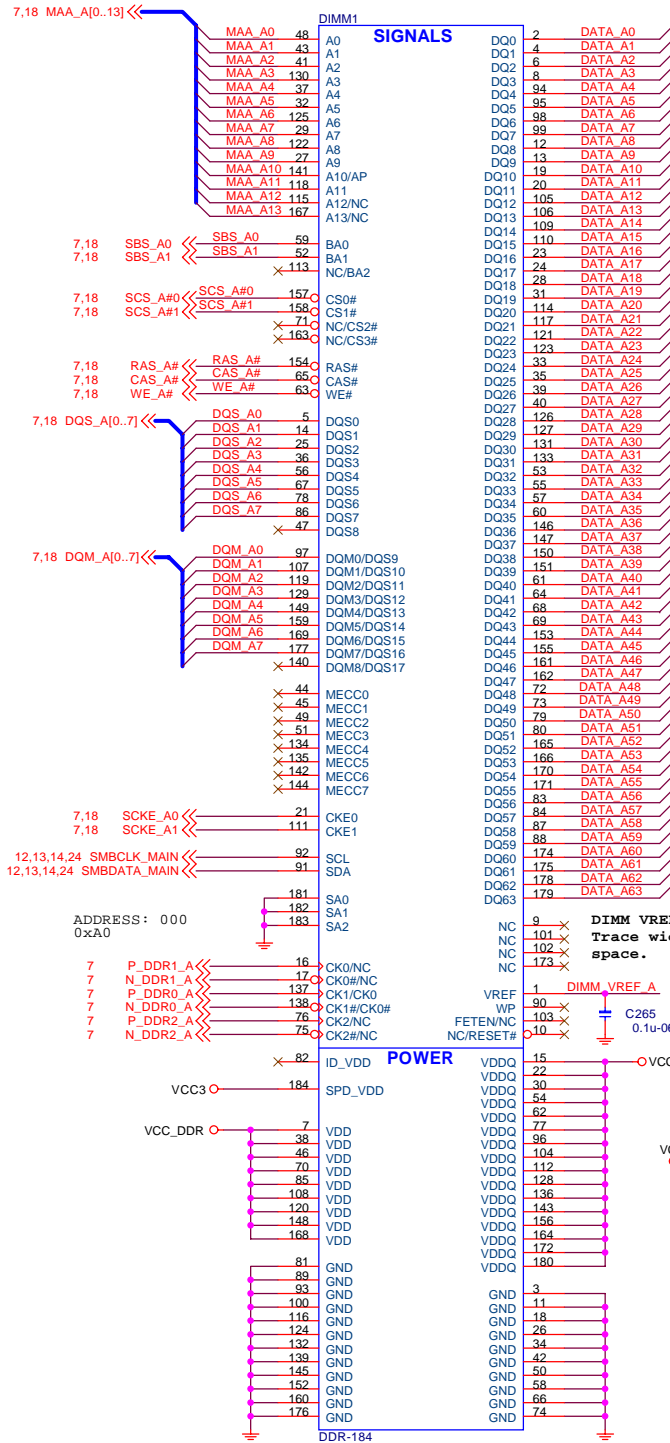


Channel A

DDR DIMM1

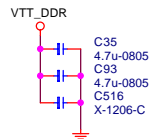
Channel B

DDR DIMM2

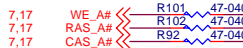
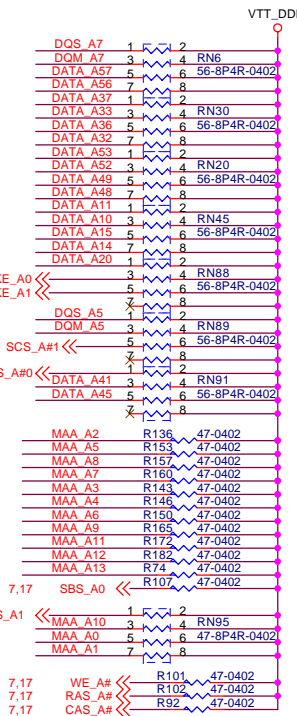
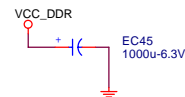
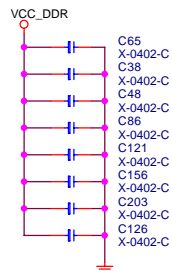
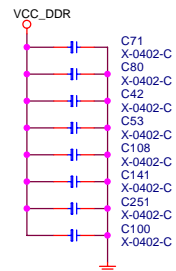
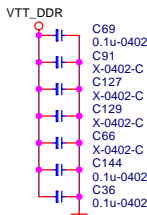
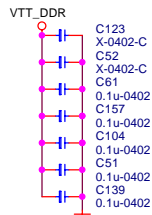
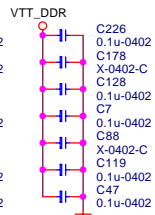
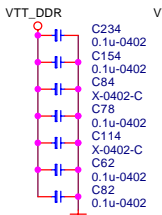
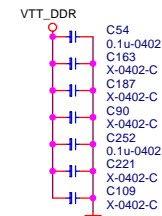
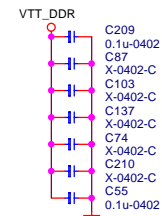
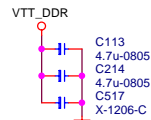


MICRO-STAR IN'L CO., LTD.		Engineer Shun Min Hsu
Title DDR DIMM 1 & 2		Drawn by Shun Min Hsu
Size Custom	Project Name MS-7085	Rev B
Date: 2004/09/03	Sheet 17	of 27

PLACED AT LEFT AND RIGHT ENDS OF
VTT ISLAND

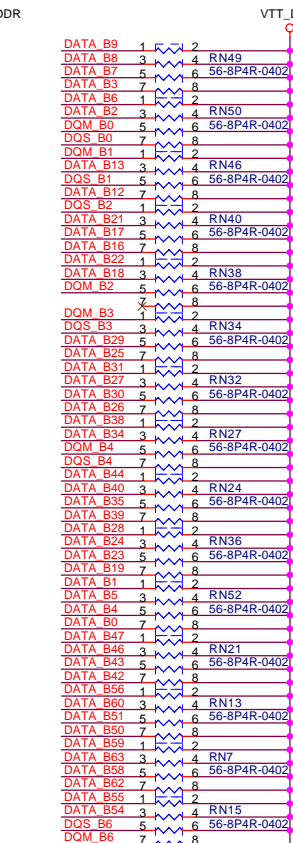
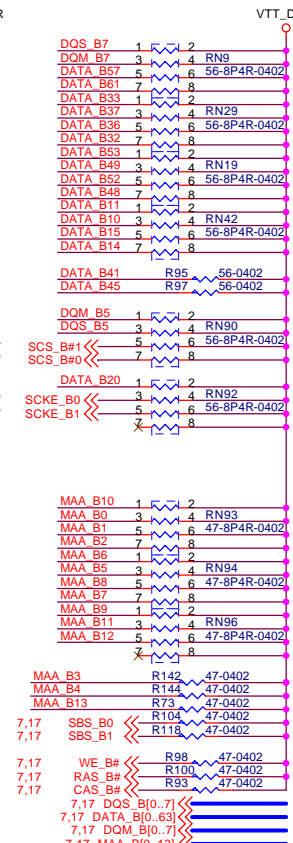
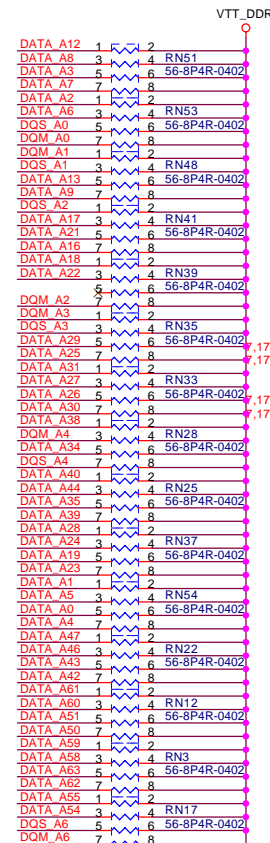
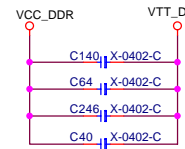


PLACED AT LEFT AND RIGHT ENDS OF
VTT ISLAND



Data Group: SDQS,SDQ & SDM (56 ohm)
Control Group: SCS# & SCKE (56 ohm)
Command Group: SMA,SBS,SRAS#SCAS# & SWE# (47 ohm)

For EMI request



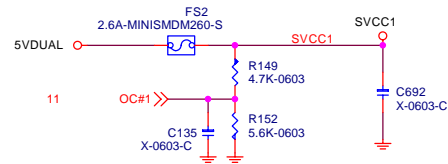
Data Group: SDQS,SDQ & SDM (56 ohm)
Control Group: SCS# & SCKE (56 ohm)
Command Group: SMA,SBS,SRAS#SCAS# & SWE# (47 ohm)

MICRO-STAR INT'L CO., LTD.

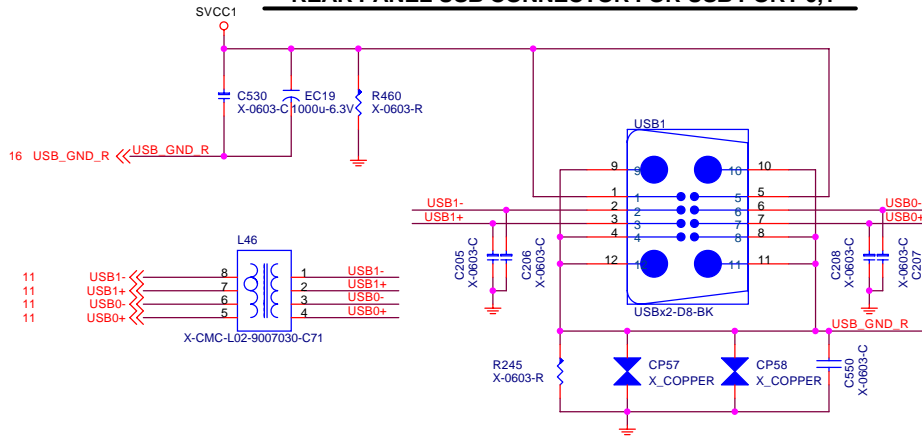
Title		DDR Termination Resistors	
Size	A3	Project Name	MS-7085
Date:	2004/09/03	Sheet	18 of 27

Engineer
Shun Min Hsu
Drawn by
Shun Min Hsu

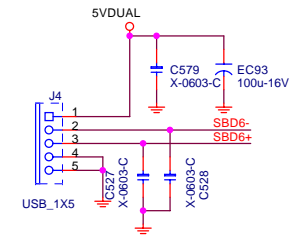
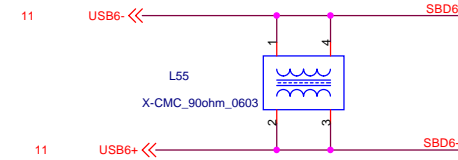
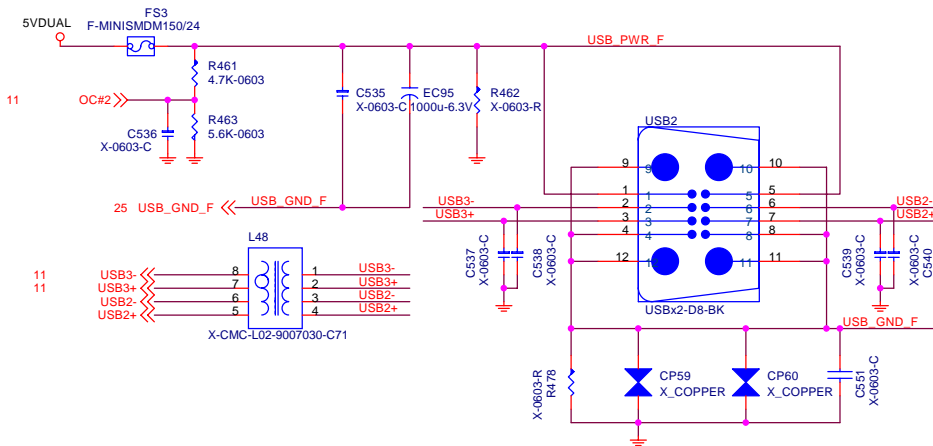
POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)



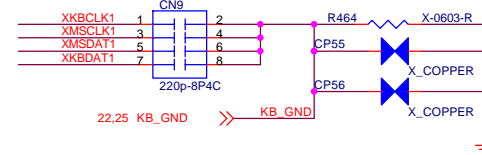
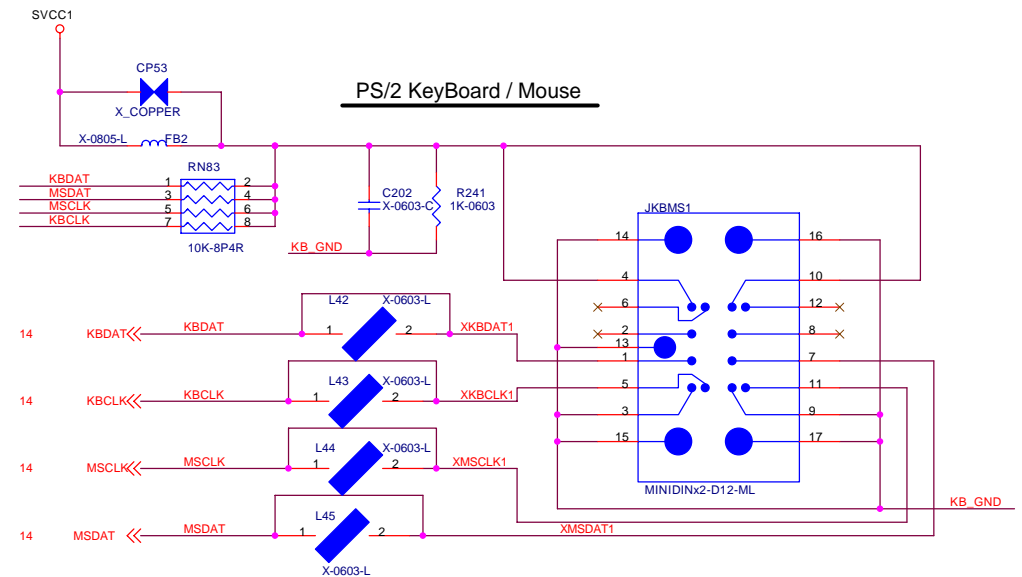
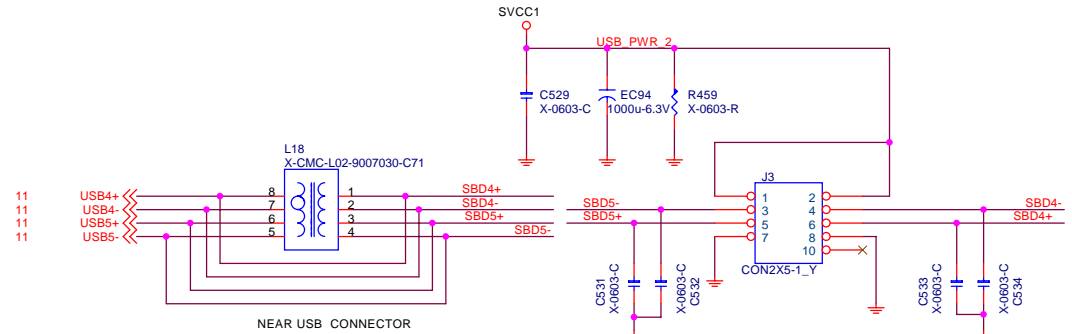
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



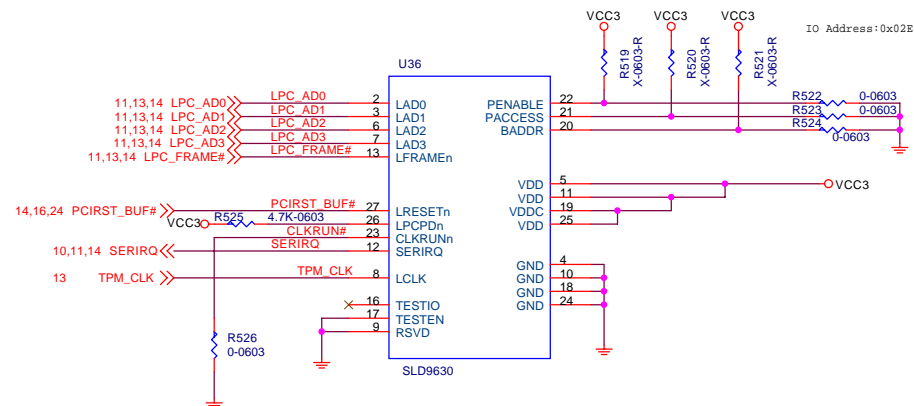
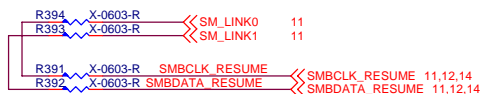
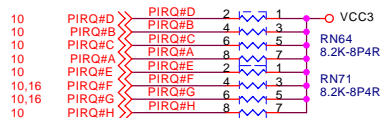
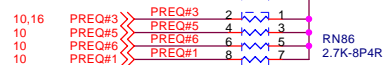
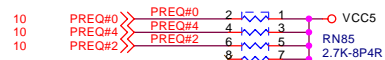
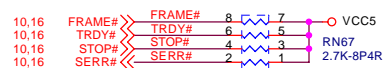
J4 only for PCMCIA



MICRO-STAR INT'L CO., LTD.

Title		Engineer	
USB CONNECTORS and PS2		Shun Min Hsu	
Size		Drawn by	
A3		Shun Min Hsu	
Project Name		Rev	
MS-7085		(B)	
Date:		Sheet	
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PCI PULL-UP / DOWN RESISTORS



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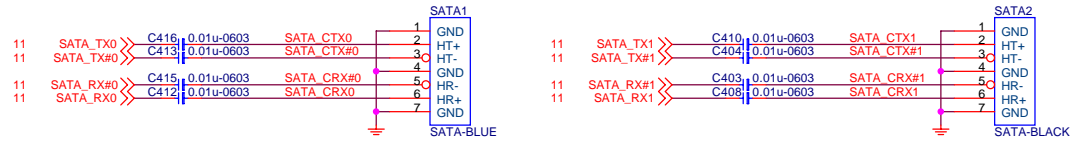
Engineer
Shun Min Hsu
Drawn by
Shun Min Hsu

PCI PULL-UP RESISTORS and TPM

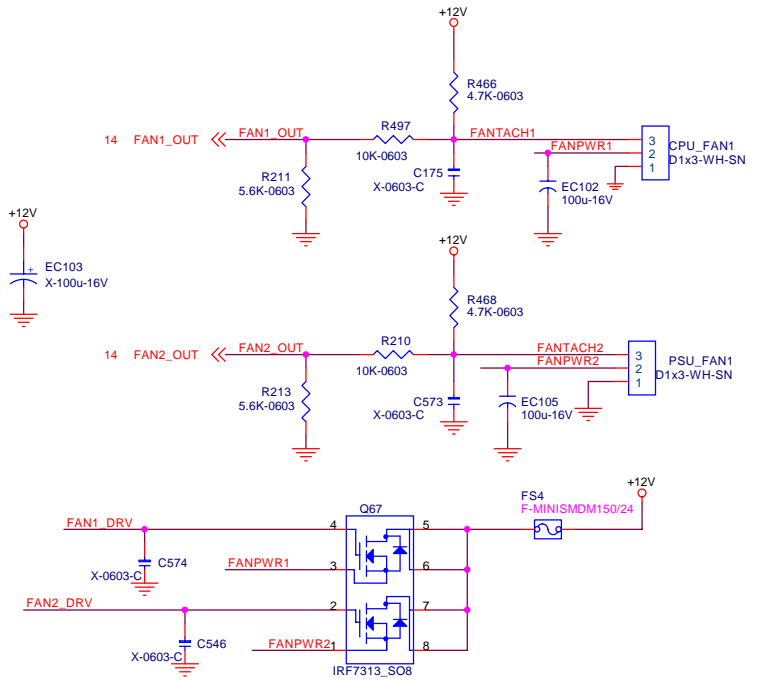
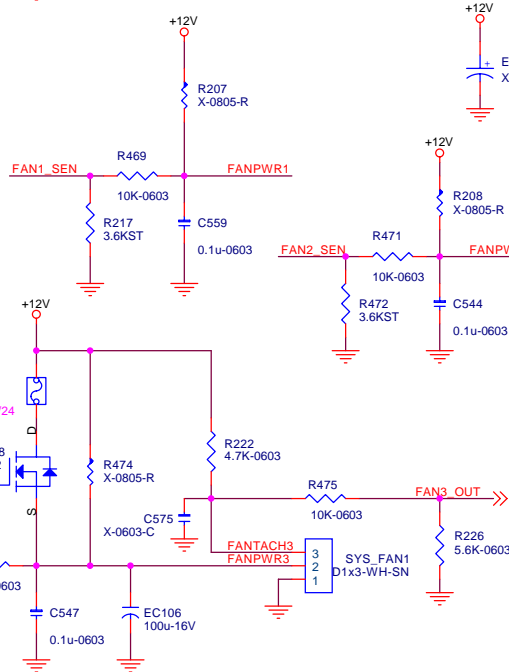
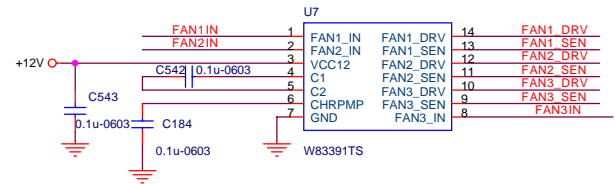
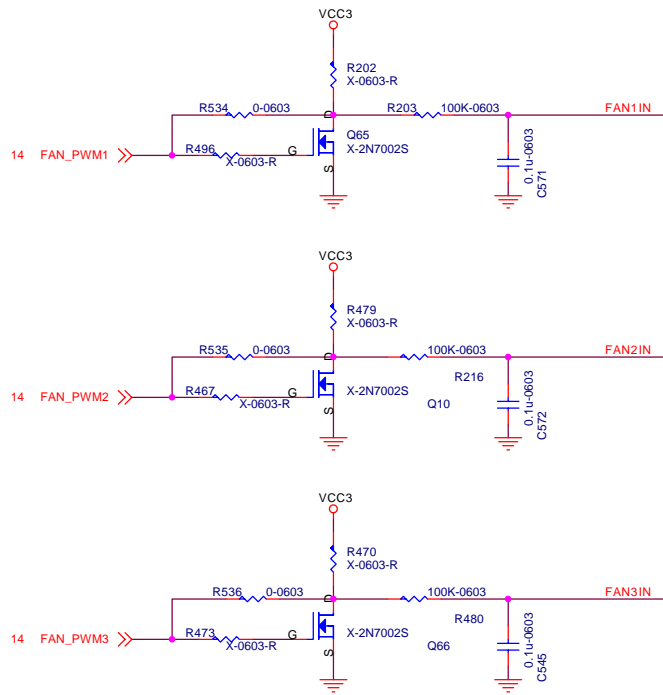
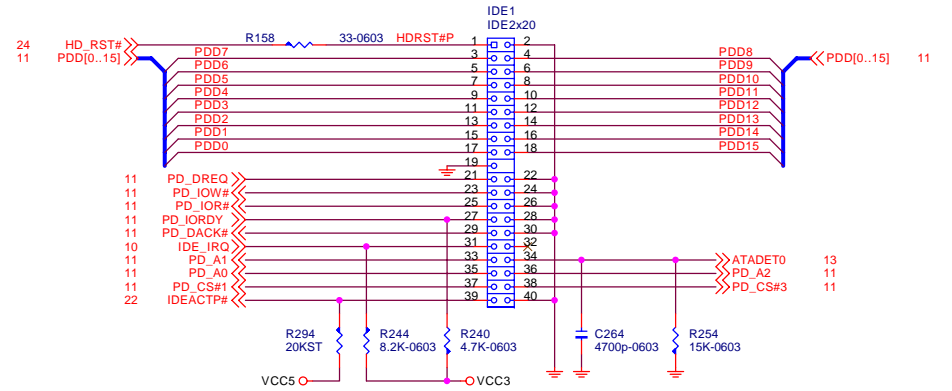
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SERIAL ATA CONNECTOR BLOCK

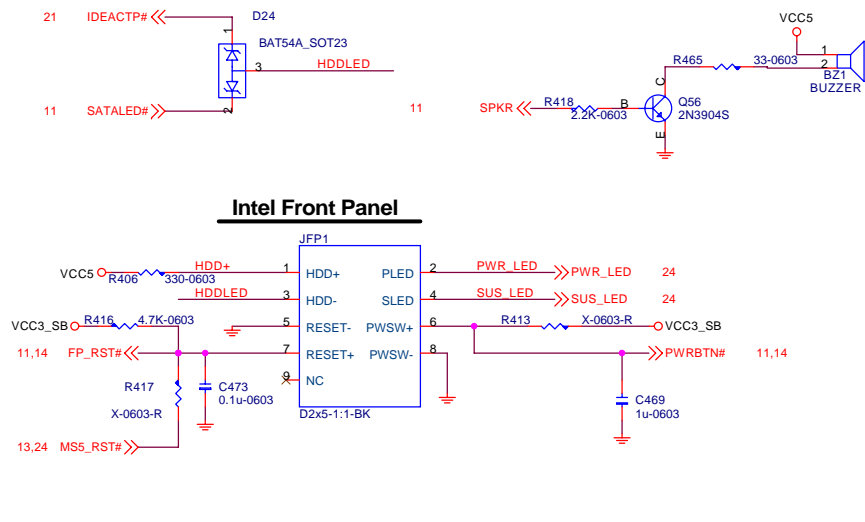


ATA 33/66/100 IDE Connectors

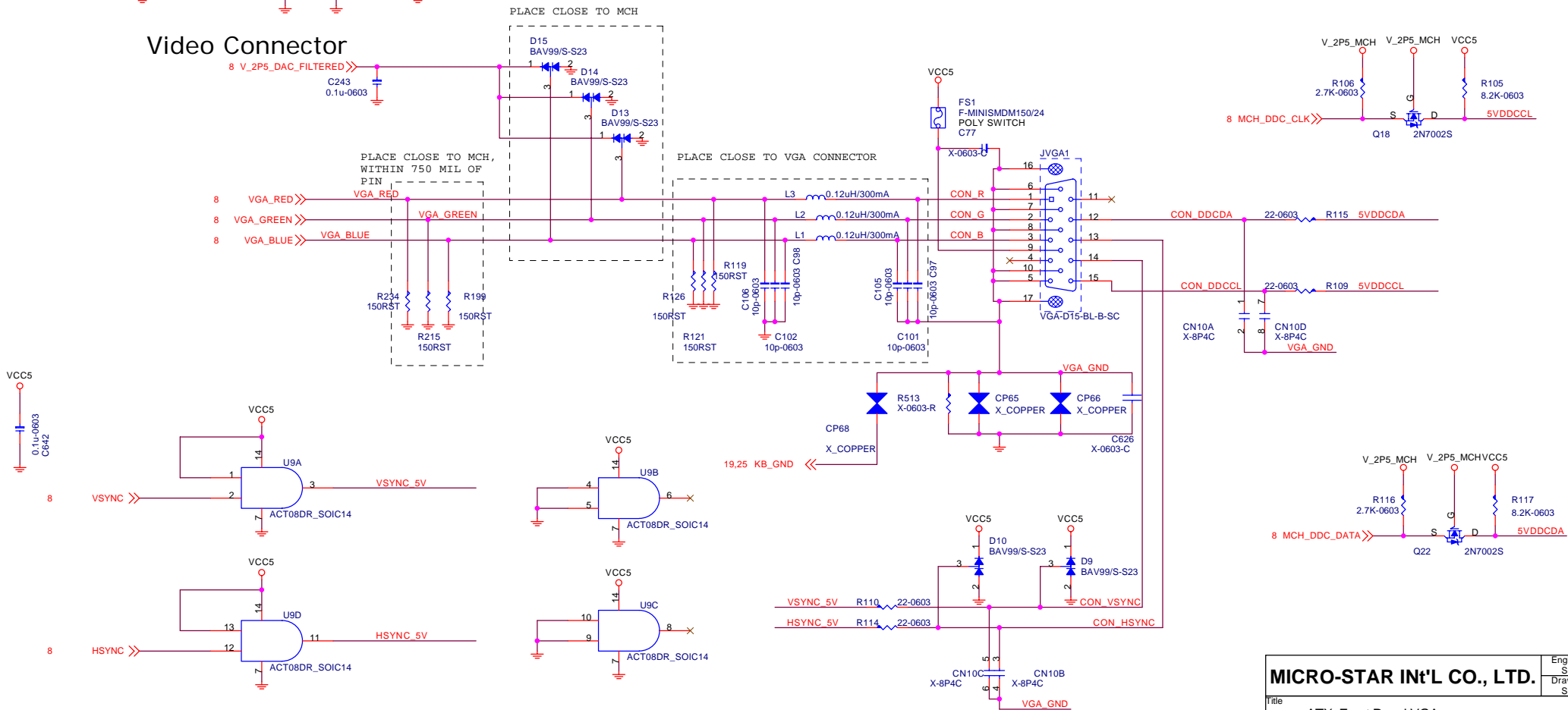


MICRO-STAR INT'L CO., LTD.				Engineer Shun Min Hsu	
Title				Shun Min Hsu	
SATA1,2 , IDE1& Fan control					
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ATX Connector



Video Connector

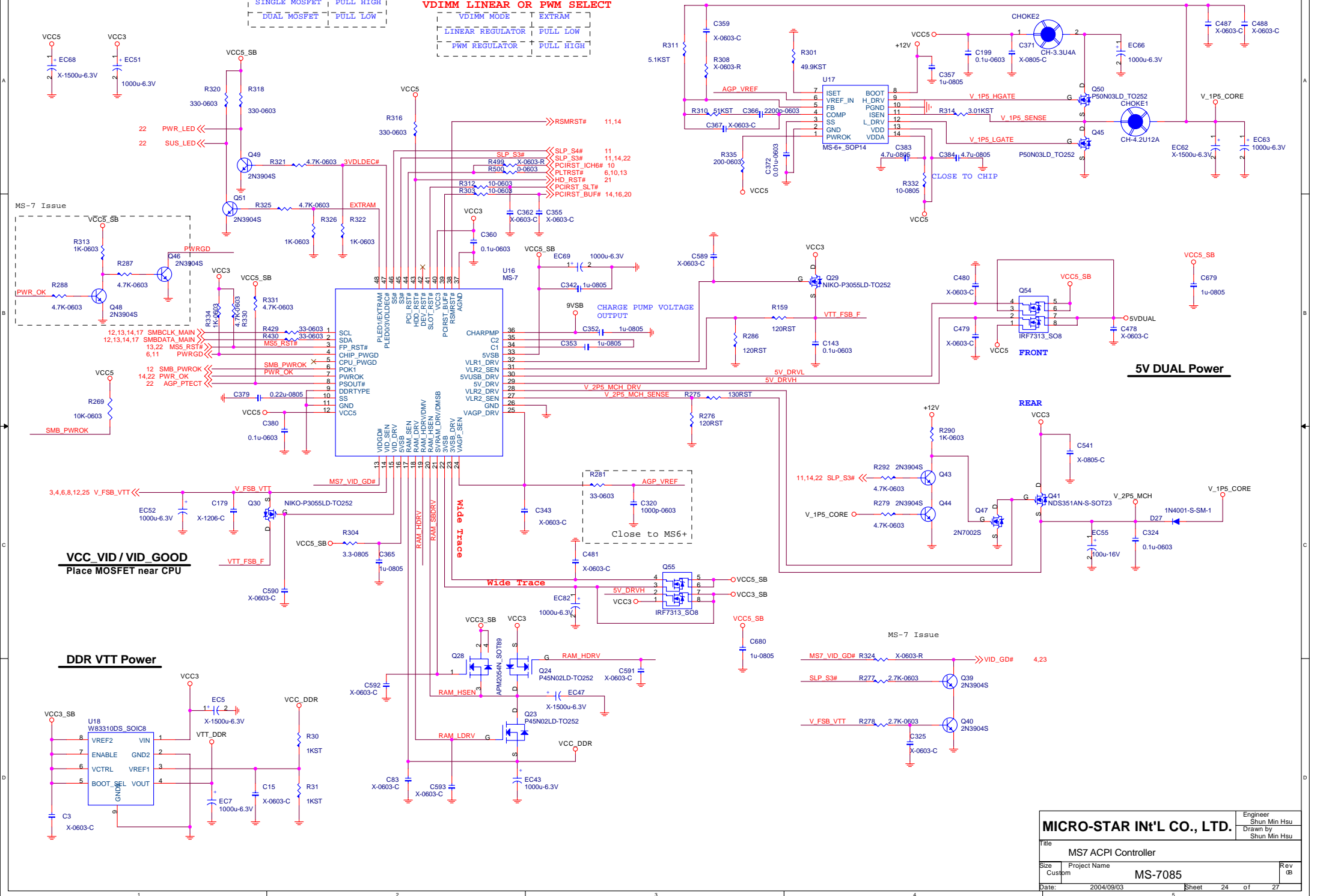


ACPI Controller

3VSB MODE SELECT
 3VSB MODE 3VLDDEC#
 SINGLE MOSFET PULL HIGH
 DUAL MOSFET PULL LOW

VDIMM LINEAR OR PWM SELECT
 VDIMM MODE EXTRAM
 LINEAR REGULATOR PULL LOW
 PWM REGULATOR PULL HIGH

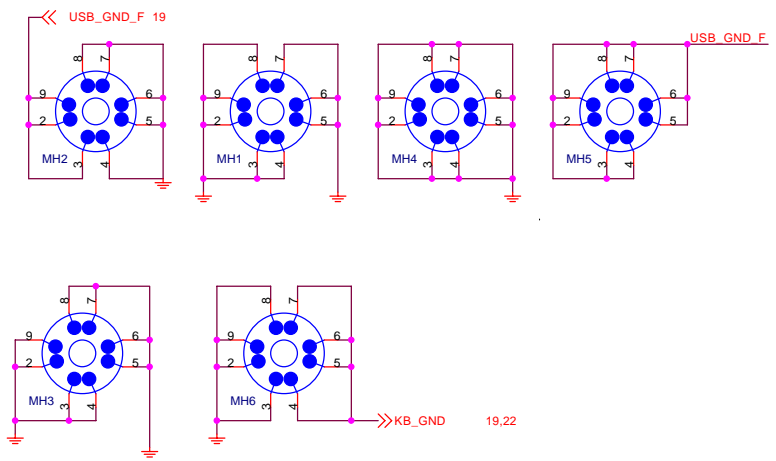
AGP POWER



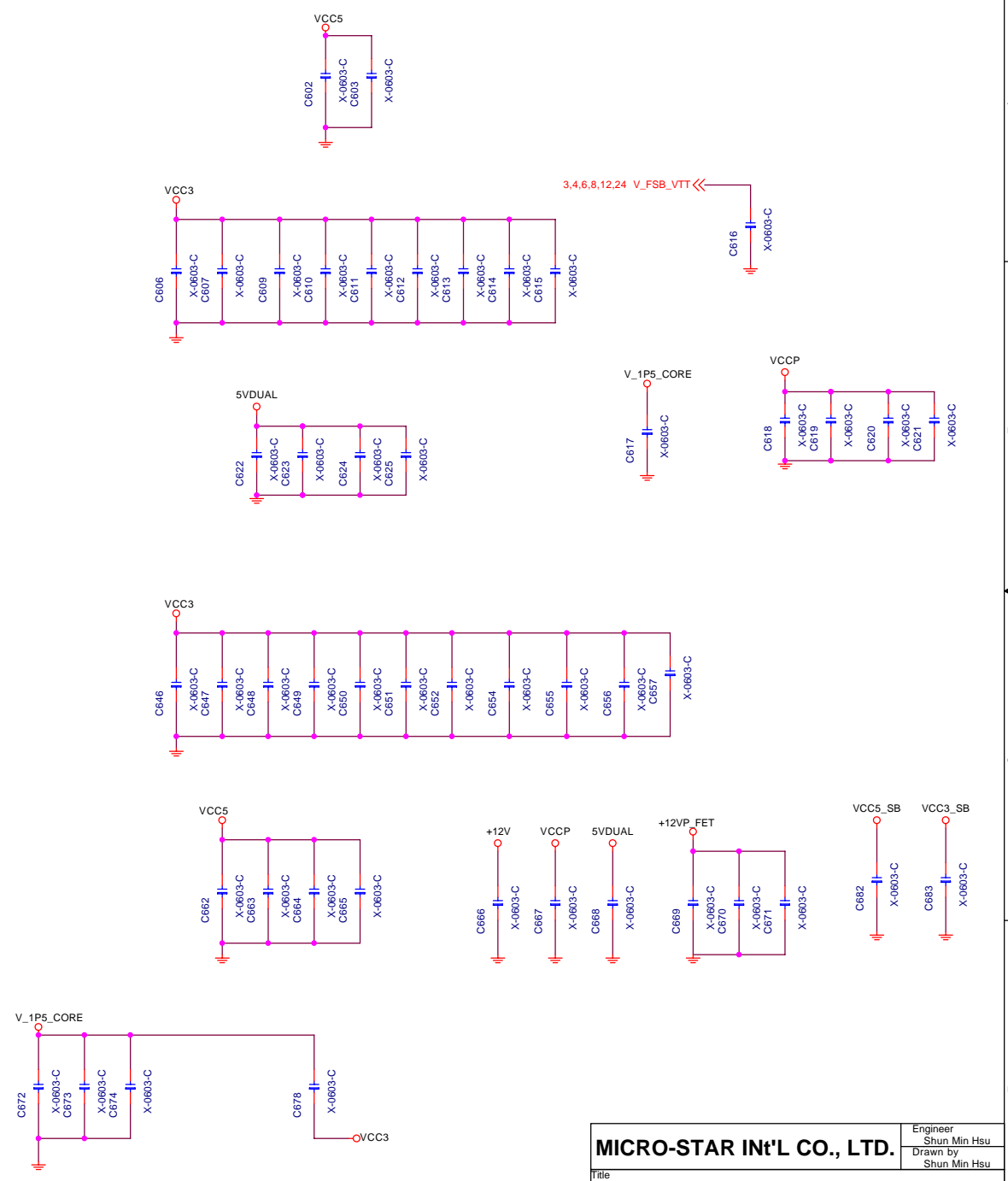
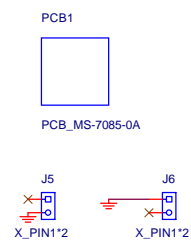
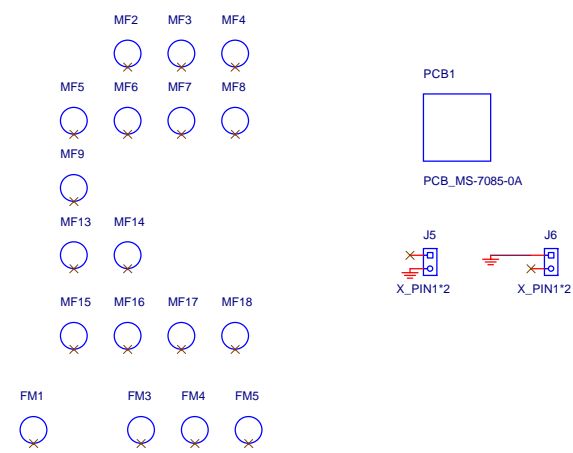
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Title		MS7 ACPI Controller	
Size		Project Name	
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Engineer
Shun Min Hsu
Drawn by
Shun Min Hsu



for EMI



MICRO-STAR INT'L CO., LTD.		Engineer Shun Min Hsu	
Title Misc		Drawn by Shun Min Hsu	
Size A3	Project Name MS-7085	Rev (B)	
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PCI Config.

DEVICE	BUS#	Device#	Function	IDSEL	INT Routing	REQ# /GNT#	CLK GEN PIN OUT
Intel 915GV							
DDR controller	0	0	0	Internal			
Integrated Graphics	0	2	0	Internal	A		
ICH6							
PCI Bridge	0	30	0	Internal			
LPC Bridge	0	31	0	Internal			
IDE	0	31	1	Internal	C		
SATA	0	31	2	Internal			
SM Bus	0	31	3	Internal	B		
AC97 AUDIO	0	30	2	Internal			
USB UHCI 0	0	29	0	Internal	A		
USB UHCI 1	0	29	1	Internal	D		
USB UHCI 2	0	29	2	Internal	C		
USB UHCI 3	0	29	3	Internal	A		
USB 2.0 UHCI	0	29	7	Internal	H		
LAN RTL8101L				AD29	F	REQ# GNT#3	PIN3 (PCI_CLK4)
PCI SLOT				AD16	A	REQ# GNT#1	PIN2 (PCI_CLK3)

ICH6 GPIO

GPIO Pin	Type	Function	Tolerance	Power
GPI 0	I	REQ6#	5V	Core
GPI 1	I	REQ5#	5V	Core
GPI 2	I	PIRQE#	5V	Core
GPI 3	I	PIRQF#	5V	Core
GPI 4	I	PIRQG#	5V	Core
GPI 5	I	PIRQH#	5V	Core
GPI 6	I	Unused	3.3V	Core
GPI 7	I	Unused	3.3V	Core
GPI 8	I	Unused	3.3V	Resume
GPI 9	I	USB_OC4#	3.3V	Resume
GPI 10	I	USB_OC5#	3.3V	Resume
GPI 11	I	SMB_ALERT#	3.3V	Resume
GPI 12	I	Unused	3.3V	Core
GPI 13	I	SIO_PME#	3.3V	Resume
GPI 14	I	USB_OC6#	3.3V	Resume
GPI 15	I	USB_OC7#	3.3V	Resume
GPO 16	O	GNTA#/Unused	3.3V	Core
GPO 17	O	GNTB#/Unused	3.3V	Core
GPO 18	O	Unused	3.3V	Core
GPO 19	O	BIOS_WP#	3.3V	Core
GPO 20	O	Unused	3.3V	Core
GPO 21	O	Unused	3.3V	Core
GPIO 22	N/A	N/A	N/A	N/A
GPO 23	O	Unused	3.3V	Core
GPIO 24	I	SIO SMI#	3.3V	Resume
GPIO 25	O	Strap pin for VCC2_5 regulator	3.3V	Resume
GPI 26	I/O	Unused	3.3V	Core
GPIO 27	I/O	Unused	3.3V	Resume
GPIO 28	I/O	Unused	3.3V	Resume
GPI 29	I	Unused	3.3V	Core
GPI 30	I	Unused	3.3V	Core
GPI 31	I	Unused	3.3V	Core
GPIO 32	I/O	Unused	3.3V	Core
GPIO 33	I/O	Unused	3.3V	Core
GPIO 34	I/O	Unused	3.3V	Core
GPIO39:35	N/A	N/A	N/A	N/A
GPI 40	I	REQ#4	5V	Core
GPI 41	I	LRDQ1#/Unused	3.3V	Core
GPIO47:42	N/A	N/A	N/A	N/A
GPIO 48	O	GNT4#/Unused	3.3V	Core
GPIO 49	OD	CPUPWEGD	V_CPU_IO	Core

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Engineer
Shun Min Hsu

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Title

PCI configuration and GPIO

Size

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Change Note

Ver:0A

2004/07/02

- 1. page13: nopop Q31 Q32 Q33 level shift circuit and change RN77 to 0R
Reserve R508 for VTT_PWRGD# signal
- 2. page20: remove mini-PCI slot
- 3. page23: modify the quantities of bulk caps and MOS
- 4. page24: Remove RAM_HDRV/RAM_HDRV1 circuit.
Modify V_2P5_MCH power sequencing circuit
- 5. page11: SATA2 connect to ICH6 port2
- 6. page12: nopop SM BUS isolation circuit
- 7. page14: connect SMBUS to SIO pin104 and pin105
- 8. page15: Add mute circuit
- 9. page24:Reserve 0603 caps on the GATE of Q30 Q28 Q24 Q23 Q29
- 10. page25: Reserve Caps for EMI

2004/07/12

- 1. page8: Add R517 R516 39.20hm on HSYNC and VSYNC.
- 2. page11: change WAKE# pull-up to VCC3_SB through a 1k ohm resistor.
- 3. page4: Modify CPU VCCA filter circuit.

2004/07/15

- 1. page15: R379 R380 change to nopop.
- 2. page20: Add TPM circuit.
- 3. page10: Reserve R527 for PCI_PME# pullup

2004/07/28

- 1. page26: Add PCI Configuration and GPIO

Ver:0B

2004/08/18

- 1. page14: Swap KBRST# and A20GATE ---- connect to wrong pins on 0A
- 2. page13: Change RN77 to 10Kohm ---- to fix U14 pin51 can not output clock
- 3. page 22: Add R529 on SLP_S3# ---- to avoid SLP_S3#=0.7V when SLP_S3#-->high

2004/08/23

- 1. page21: change CPU FAN connector and add SYSTEM FAN-- For thermal request
- 2. page20: Remove PCI slot -- For thermal request
- 3. page14: Disconnect SIO pin111 and ICH6 pinW6 --- to fix auto power-on issue

2004/08/26

- 1. page14: Change HVCC to VCC3_SB and RN70 connect to VCC3_SB----- For auto power-on problem
- 2. page19: Change J4 to PCMCIA connector ---NEC request
- 3. page13: Add JLPC1 for Debug

2004/08/30

- 1. page22: Reserve C686 C687 C688 C690 For EMI
- 2. page19: Reserve C692 For EMI

2004/08/31

- 1. page14: add RN79 R538 pull up to VCC3_SB because VID[0-4] are input pins

2004/09/03

- 1. page21: add FS4 FS5 on fan control circuit for safety
- 2. page21: change R497 R210 R475 to 10K
change R211 R213 R226 to 5.6K --- adjust FANTACH voltage level to 3V

MICRO-STAR INT'L CO., LTD.		Engineer Shun Min Hsu	
Title Change Note		Drawn by Shun Min Hsu	
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